Efficient FPGA Implementation of a Variable Digital Filter based Spectrum Sensing Scheme for Cognitive IoT Systems

Abhishek Ambede, A. P. Vinod
School of Computer Science and Engineering,
Nanyang Technological University (NTU),
Singapore 639798.
abhishek7@e.ntu.edu.sg, asvinod@ntu.edu.sg

Shanker Shreejith
School of Engineering,
University of Warwick,
Coventry, CV47AL, United Kingdom.
s.shanker@warwick.ac.uk

***Abstract*— Wireless communication in Internet of Things (IoT) systems involves several devices communicating in the limited available frequency spectrum using different wireless communication standards. To achieve efficient spectrum usage in the IoT systems, it is desired to have the ability of dynamic spectrum allocation. Cognitive radios (CR) enable efficient spectrum utilization by performing spectrum sensing to gain the knowledge of current spectrum occupancy and dynamically reconfiguring the communication parameters, making them highly suitable for IoT systems. In this paper, we present the efficient hardware implementation of a spectrum sensing scheme for CR based IoT applications that require large bandwidth. We show that the proposed implementation on field programmable gate arrays (FPGAs) can achieve over 1.56x improvement in performance, while consuming 77% less generic resources and at a fractionally higher power consumption.**

***Index Terms*— Internet of things; cognitive radio; spectrum sensing; variable digital filters; FPGA; pipelining.**

I. Introduction

Cognitive radios (CRs) feature the ability to monitor the spectrum utilization in real-time and adapt their transmission and reception parameters dynamically to perform opportunistic spectrum usage [1, 2]. CR based wireless communication systems can thus achieve efficient spectrum utilization. Recent research envisions CR as an enabling technology for realizing spectrally efficient Internet of Things (IoT) systems [3]. Wireless communication in IoT systems involves multiple sensors and devices communicating using different standards such as Bluetooth, ZigBee, Wi-Fi and others. Due to limited availability of the radio frequency spectrum, it is difficult to realize such multi-standard IoT systems using static spectrum allocation techniques. The ability of CRs to perform opportunistic spectrum usage can enable dynamic spectrum allocation for the communicating nodes in the IoT systems, thereby leading to high spectral efficiency. Therefore, CRs are highly suitable candidates to realize IoT systems.

An important function in CRs is spectrum sensing, wherein the presence or (and) absence of signals of licensed users is to be detected in the wideband input frequency range in order to allow opportunistic access of the vacant frequency bands to unlicensed users (called CR users) [4]. The vacant frequency bands are termed as spectrum holes. Out of the various techniques used for spectrum sensing in CRs, the energy detector based spectrum sensing is the least complex to implement [4]. In this technique, variable digital filters (VDFs) or filter banks can be used to detect spectrum holes by comparing signal energy in the corresponding frequency bands with a threshold value [5]. Fig. 1 shows three different cases of frequency bands which may be sensed in an input signal – a lowpass frequency band (Case 1), a bandpass frequency band (Case 2) and a highpass frequency band (Case 3). Correspondingly, VDFs and filter banks that provide lowpass, highpass and bandpass frequency responses with variable cutoff frequencies over the entire Nyquist frequency range are used to detect spectrum holes of varying bandwidths and locations.

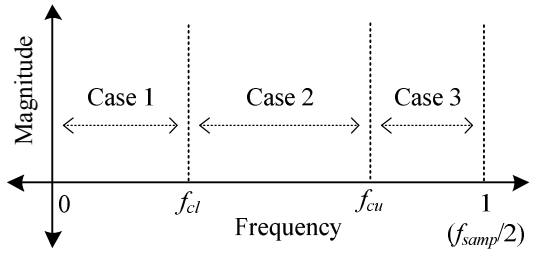

Fig. 1. Different cases for energy computation.

Various approaches have been proposed in literature to realize VDF or filter bank based spectrum sensing schemes [5-8]. We have proposed a VDF based low complexity spectrum sensing scheme in [8]. In this scheme, two VDFs providing unabridged control over cutoff frequency are used to compute energies corresponding to any of the three frequency band cases shown in Fig. 1. In this paper we focus on the efficient implementation of this spectrum sensing scheme and provide hardware implementation architectures for the VDFs on field-programmable gate array (FPGA) platforms. FPGAs are ideal candidates for CR as they allow complex computations to be accelerated in hardware and offer techniques to dynamically adapt hardware modules to support multi-standard radio or efficient shaping/spectrum sensing techniques [9]. Our

978-1-5090-5479-8/17/$31.00 ©2017 IEEE

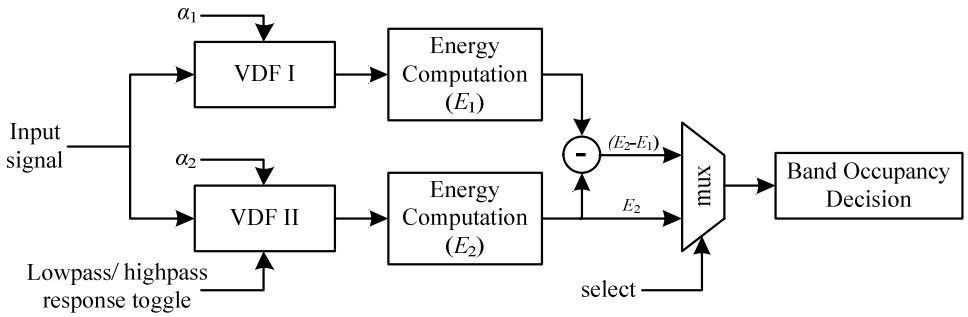

Fig. 2. Block diagram of the VDF based spectrum sensing scheme proposed in [8].

implementation results show that the proposed implementation architectures help to achieve 1.56x higher operating frequencies for the VDFs used in this scheme while consuming 77% less resources, thereby enabling its usage for large bandwidth operations on low-end FPGA devices.

The rest of the paper is organized as follows: Section II presents a brief review of the spectrum sensing scheme proposed in [8] and the corresponding challenges and motivations for the work presented in this paper. Section III presents the proposed hardware implementation architectures for our spectrum sensing scheme and describes the corresponding FPGA implementation. The implementation results along with their detailed comparative analysis are presented in Section IV. Section V presents our conclusions.

II. Related Work and Motivation

In [8], we proposed a variable digital filter (VDF) based low complexity spectrum sensing scheme. A high level block diagram of the approach in [8] is shown in Fig. 2. The technique uses two VDFs – VDF I and VDF II to perform energy detection based spectrum sensing. VDF I can be realized using the 1st order all pass transformation (APT) based filter design technique [10, 11] and can provide variable lowpass frequency responses with unabridged control over the cutoff frequency. On the other hand, VDF II is based on the combination of the improved coefficient decimation method [12] and the 1st order APT technique [10, 11]. VDF II can provide variable lowpass as well as highpass frequency responses with unabridged control over the cutoff frequency. VDF I and VDF II can be appropriately used to perform energy computation corresponding to any of the three cases shown in Fig. 1. In [8], it was shown that these VDFs are low complexity alternatives to other relevant VDFs that provide similar functionality.

Fig. 3 shows the hardware implementation architecture used to realize the two VDFs shown in Fig. 2. A single set of prototype filter coefficients is implemented using the conventional transposed direct form architecture. The two desired branches corresponding to VDF I and VDF II are realized by replacing all the delay units by the 1st order all pass filter structure shown in Fig. 4. The two warping coefficients α_1 and α_2 are used to control the resultant cutoff frequencies obtained from the two VDF branches. The corresponding mathematical formulation for computing the values of α_1 and α_2 has been provided in [8]. In the VDF II branch, alternate

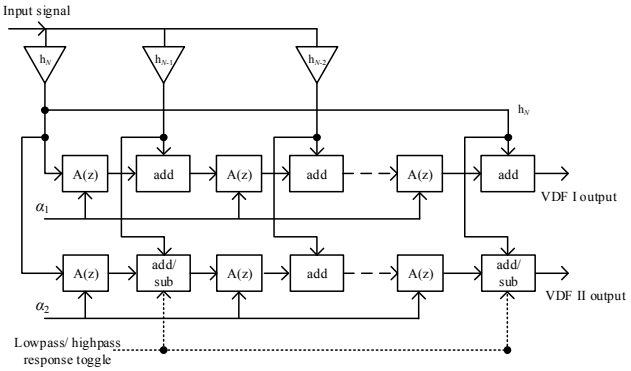

Fig. 3. Hardware implementation architecture for VDF I and VDF II shown in Fig. 2.

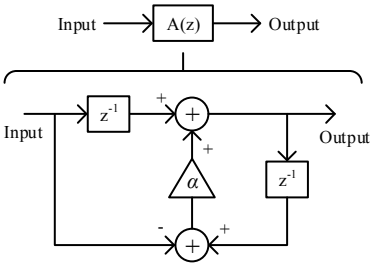

Fig. 4. Hardware implementation architecture for 1st order all pass filter.

adder blocks are replaced by adder/ subtractor blocks to enable the lowpass to highpass toggle operation which is based on the improved coefficient decimation method.

If the conventional hardware implementation architectures shown in figures 3 and 4 are used to realize the spectrum sensing scheme, it is observed that the resultant VDFs face severe limitations with their operating frequencies. This is due to the inherent disadvantage of the APT based VDF I and VDF II that are implemented using these conventional architectures – long critical paths resulting in low values of maximum operating frequency. As a result, only low operating speeds are possible for this spectrum sensing scheme thereby limiting its scope to low bandwidth CR applications. In this paper, we address these drawbacks and propose modified hardware implementation architectures to achieve high speed realizations of the two VDFs. The subsequent sections present our modified hardware implementation architectures and the detailed comparative analysis using corresponding FPGA implementation results.

III. Proposed Implementation of the Spectrum Sensing Scheme

A. Proposed Implementation Architectures

The conventional hardware implementation architectures proposed for the two VDFs in the spectrum sensing scheme are shown in figures 3 and 4. As discussed in Section II, direct hardware implementation of these architectures severely limits the operating speed of the two VDFs, limiting their scope to low bandwidth applications. To address this drawback and enable the realization of high speed VDFs for the spectrum sensing scheme, we present modified implementation architectures. The modified implementation architectures are shown in figures 5 and 6. When compared with the conventional architectures in figures 3 and 4, it can be observed that the modified architectures contain additional delay elements. These delay elements are used to break the critical path of the implementation architecture into short uniform length sections. This pipelined implementation of the two VDFs constraints the critical path to be between the two adders and a multiplier that occur in series within the all pass filter block. This constant critical path can be observed in the proposed pipelined implementation architecture for 1st order all pass filter shown in Fig. 6.

The pipelined architectures also allow the critical path to be independent of the prototype filter order, enabling complex higher order filters to be implemented with nearly identical performance. Thus, the proposed implementation architectures enable the usage of the spectrum sensing scheme for large bandwidth operations. It is to be noted that the pipelined implementation architectures have a higher latency than their conventional counterparts due to the additional delay elements. But this is a negligible disadvantage as it only leads to a small initial delay at the VDF output.

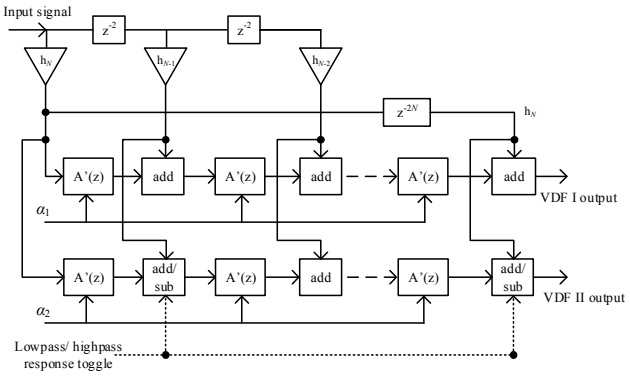

Fig. 5. Pipelined hardware implementation architecture for VDF I and VDF II shown in Fig. 2.

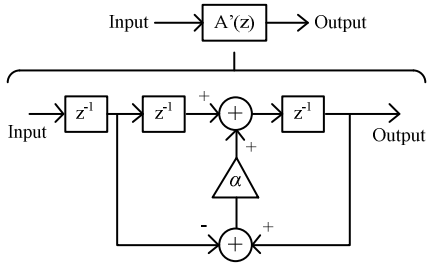

Fig. 6. Pipelined hardware implementation architecture for 1st order all pass filter.

B. FPGA Implementation

In this section we present a design example to compare the FPGA implementation results of the spectrum sensing scheme realized using the conventional and proposed implementation architectures, and explore optimizations to implement them efficiently on modern FPGAs. Consider a design example wherein the spectrum sensing scheme is realized using a halfband prototype filter with the following specifications - passband and stopband peak ripple specifications as 0.05 dB and -45 dB respectively, normalized transition bandwidth 0.1. The order of the prototype filter is computed to be 48 and its coefficients are obtained using MATLAB. As the prototype filter is halfband and the spectrum sensing scheme's implementation architectures are based on the transposed direct form architecture, only 1/4th of the prototype filter coefficients need to be implemented.

To implement this filter in an efficient manner while offering the high performance required for IoT systems, we make use of the DSP blocks available on modern FPGAs. We have chosen the Zynq hybrid FPGA platform from Xilinx as it enables the cognitive software and computational hardware to be tightly coupled for advanced software defined radio applications while offering software-driven reconfigurability [9]. While pipelining improves the overall performance of the VDF, direct implementation of the architecture results in sub-optimal utilisation of the DSP blocks, increased resource consumption and lower performance. Also, direct implementations are unable to explore specific architectural capabilities, resulting in large wastage of generic FPGA resources like Look-Up Tables (LUTs) and Flip-Flops (FFs).

In our optimised implementation, we map each all pass filter shown in Fig. 6 into a single DSP block on the Zynq device (DSP48E1 block). This allows us to absorb all the delay registers in the pipelined all pass filter into the internal registers of the DSP block to achieve maximum operating frequency. Further, consecutive all pass filter blocks that are encountered due to the usage of a halfband prototype filter (alternate filter coefficients are '0') allows the DSP blocks to be chained using dedicated routing, improving the data-path delay between consecutive all pass filter blocks. These manual optimisations enable a compact implementation of the two VDF consuming minimum generic resources (like LUTs and FFs), while offering enough resources to implement other baseband modules on the same FPGA. We also explicitly map the coefficient multipliers to the DSP blocks using direct instantiation, leaving aside generic resources for implementing other baseband modules in the radio system.

IV. Results

To evaluate the performance of the optimised VDFs for detecting spectrum holes in multi-standard IoT systems, we use the example scenario that was shown in Fig. 1. Fig. 7 illustrates

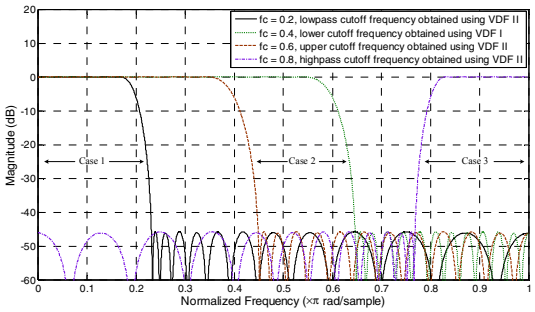

Fig. 7. Frequency responses obtained using VDF I and VDF II in the spectrum sensing scheme.

the three types of frequency responses obtained using the proposed VDF I and VDF II. It can be noted that VDF I provides lowpass frequency responses corresponding to the lower cutoff frequencies in Case 2, whereas VDF II provides lowpass frequency responses corresponding to the upper cutoff frequencies in Case 2 as well as lowpass and highpass frequency responses corresponding to Case 1 and Case 3 respectively. It is to be noted that the two VDFs provide unabridged cutoff frequency control over the entire Nyquist frequency range.

We compare our optimized implementation of the pipelined VDFs against two scenarios: a non-pipelined implementation and a pipelined sub-optimal implementation on the same Zynq 7z020 device, the results of which are shown in Table 1. The sub-optimal implementation results from a direct mapping of the pipelined VDF architecture. All implementation runs were configured to make use of the DSP blocks available on the Zynq device to improve their performance. It can be observed that the non-pipelined design and the sub-optimal pipelined design consumes more LUTs and FFs than our optimized design since it maps the registers and adders in the all pass filter to these resources. The optimizations also enable our design to achieve 1.56x higher operating frequency than the pipelined design (and 67x higher than non-pipelined implementation), while consuming 77% less resources, enabling compact implementations possible on low-power FPGAs.

We also measure the power consumption of the pipelined models at 100 MHz under the same activity conditions, using the XPower Analyser tool from Xilinx. It was observed that the sub-optimal pipelined design consumed 247 mW dynamic power, while the proposed design consumed a marginally higher 269 mW (dynamic power) at the same frequency. The increased power consumption of the proposed design is because the optimized mapping utilizes all 3 compute stages of the DSP block for implementing the all pass filter, compared to the multiplier-only mode in the pipelined design. Also, the proposed design can operate at much higher clock speeds if required, allowing its performance to be scaled according to the system requirements.

TABLE I. RESOURCE CONSUMPTION AND PERFORMANCE ACHIEVED ON THE XILINX ZYNQ 7Z020 DEVICE.

Design	LUTs	FFs	DSPs	F_{Max} (MHz)
Non-pipelined	8875	3590	104	2.34
Pipelined (sub-optimal)	9574	7567	104	101.5
Pipelined (optimal)	2158	2991	109	158.7

V. CONCLUSIONS

In this paper, we presented the efficient hardware implementation of a spectrum sensing scheme which can be used in CR based IoT applications. The optimisations in the implementation architectures enabled us to achieve considerably higher operating performance and resource savings over traditional pipelined implementations, at a small cost of fractionally higher power consumption, making them ideally suited for compact IoT applications.

REFERENCES

[1] J. Mitola and G. Q. Maguire, "Cognitive radio: Making software radios more personal," IEEE Pers. Commun., vol. 6, no. 4, pp. 13-18, Aug. 1999.

[2] S. Haykin, "Cognitive radio: Brain-empowered wireless communications," IEEE J. Sel. Areas Commun., vol. 23, no. 2, pp. 201-220, Feb. 2005.

[3] Q. Wu et al., "Cognitive internet of things: A new paradigm beyond connection," IEEE Internet Things J., vol. 1, no. 2, pp. 129-143, Apr. 2014.

[4] T. Yucek and H. Arslan, "A survey of spectrum sensing algorithms for cognitive radio applications," IEEE Commun. Surveys Tuts., vol. 11, no. 1, pp. 116-130, 1st Quarter 2009.

[5] B. Farhang-Boroujeny, "Filter bank spectrum sensing for cognitive radios," IEEE Trans. Signal Process., vol. 56, no. 5, pp. 1801-1811, May 2008.

[6] R. Mahesh and A. P. Vinod, "A low-complexity flexible spectrum-sensing scheme for mobile cognitive radio terminals," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 58, no. 6, pp. 371-375, Jun. 2011.

[7] S. Dikmese, P. C. Sofotasios, T. Ihalainen, M. Renfors and M. Valkama, "Efficient Energy Detection Methods for Spectrum Sensing Under Non-Flat Spectral Characteristics," IEEE J. Sel. Areas Commun., vol. 33, no. 5, pp. 755-770, May 2015.

[8] A. Ambede, K. G. Smitha and A. P. Vinod, "Low complexity spectrum sensing using variable digital filters for cognitive radio based air-ground communication," IEEE Intnl. Wkshp. Cogn. Cellular Syst., pp. 1-5, Rhine River, Germany, 2-4 Sep. 2014.

[9] S. Shreejith, B. Banarjee, K. Vipin and S. A. Fahmy, "Dynamic cognitive radios on the Xilinx Zynq hybrid FPGA", IEEE CROWNCOM, pp. 427-437, 21-23 Apr. 2015.

[10] A. G. Constantinides, "Spectral transformations for digital filters," Proc. Inst. Electr. Engineers, vol. 117, no. 8, pp. 1585-1590, Aug. 1970.

[11] S. K. Mitra and K. Hirano, "Digital all-pass networks," IEEE Trans. Circuits Syst., vol. 21, no. 5, pp. 688-700, Sep. 1974.

[12] A. Ambede, K. G. Smitha and A. P. Vinod, "A low complexity uniform and non-uniform digital filter bank based on an improved coefficient decimation method for multi-standard communication channelizers," Circuits Syst. Signal Process., Springer, vol. 32, no. 6, pp. 2543-2557, Dec. 2013.